Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Top Layer	Copper	2.80mil		
4	Dielectric 1	FR-4 High Tg	8.00mil	4.2	
5	Signal Layer 1	Copper	1.40mil		
6	Dielectric 2	FR-4 High Tg	40.00mil	4.2	
7	Signal Layer 2	Copper	1.40mil		
8	Dielectric 3	FR-4 High Tg	8.00mil	4.2	
9	Bottom Layer	Copper	2.80mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				

DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
MIN. CLEARANCE: 0.2 mm
MIN. VIA PAD SIZE: 24 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
☐ FR-408 ☒ FR-4 High Tg ☐ OTHER _____
THICKNESS: ☒ 65 MIL (1.6mm) +/-10% ☐ OTHER _____
TOLERANCE: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/- _____
BOW & TWIST: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/- _____

DRILLING:
REFERENCE: ☒ AS SHOWN ☒ NC_DRILL FILES
PTH COPPER THICKNESS: ☒ 20-30 um ☐ OTHER _____

BOARD FINISH:
SILKSCREEN: ☒ TOP ☒ BOTTOM
SILKSCREEN COLOR: ☒ WHITE ☐ OTHER _____
SOLDER RESIST COLOR: ☒ GREEN ☐ OTHER _____
☒ MATTE ☐ SEMI-GLOSS

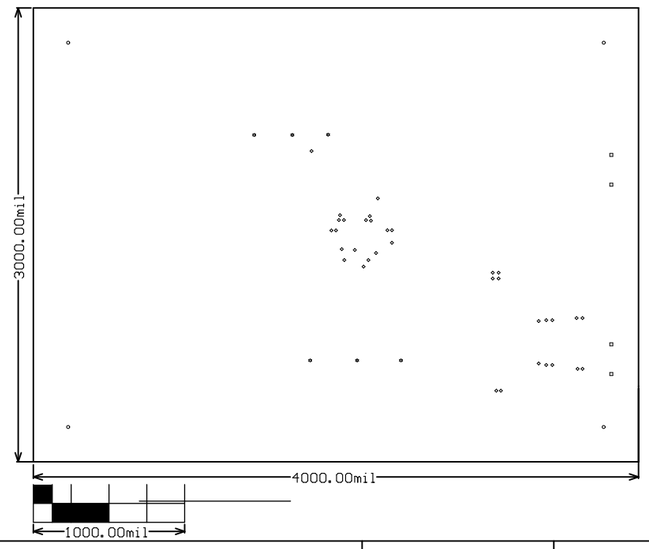
SURFACE FINISH: ☒ IMMERSION GOLD (ENIG) ☐ ENEPIG
☐ IMM. TIN/SILVER OR EQUIV ☐ OTHER _____

ARRAY/PANEL: ☐ CUT AND TRIM PER M1 BOARD OUTLINE
☐ N.C. ROUTE ☒ V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
☒ ANSI IPC-A-600F CLASS -> ☐ 1 ☒ 2 ☐ 3
☒ RoHS ☐ OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: ☐ YES
BARE BOARD ELEC. TEST: ☐ NONE ☒ REQUIRED ☐ PER ORDER
☐ XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
☐ XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
☐ OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
☐ LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE



Symbol	Quantity	Finished Hole Size	Plated	Hole Type	Drill Layer Pair	Hole Tolerance
◇	35	10.00mil (0.254mm)	PTH	Round	Top Layer - Bottom Layer	
□	4	51.18mil (1.300mm)	PTH	Round	Top Layer - Bottom Layer	
✡	6	63.00mil (1.600mm)	PTH	Round	Top Layer - Bottom Layer	
○	4	125.98mil (3.200mm)	PTH	Round	Top Layer - Bottom Layer	
	49 Total					

Note: Use the solder mask on the rest of the board on the fingers of the board. No solid gold needed.

TEXAS INSTRUMENTS

PROJECT TITLE: LM61430EVM-AS-2MHZ
DESIGNED FOR: RTM
FILE NAME: BSR195A.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: BSR195	REV: A	SVN REV: Not In VersionControl
LAYER NAME = [illegible]ions	TID #: N/A		
PLOT NAME = Fabrication Drawing	GENERATED : 6/28/2021 4:47:46 PM	TEXAS INSTRUMENTS	

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ENGINEER:	LAYOUT BY:
Marshall Beck	Marshall Beck
SCALE: 1.00	ALTIUM DESIGNER VERSION: 17.1.5.472